

Applicant: Drapkin et al.
Application No.: 09/651,944

REMARKS/ARGUMENTS

The present application contains claims 1-6, 8, 9, 11-18, 21, 24, 25, and 28 through 37. Claims 4, 11, 14-17, 21 and 24 have been withdrawn for prosecution as being directed to non-elected subject matter. Claims 7, 10, 19, 20, 22, 23, 26 and 27 have been canceled without prejudice to Applicant in order to expedite the prosecution of the present application. Claims 32-37 have been newly added.

Applicant wishes to thank Examiner Nguyen for the courtesy of granting a telephone interview and further wishes to thank the Examiner for the suggestions put forth during the course of the interview in order to expedite the prosecution of the present application.

In accordance with the Examiner's suggestions, Applicant has added, in addition to the claims previously on file, new claims 32-37 which, it is submitted further more clearly distinguish over the art of record.

For example, making reference to claim 32, there is no teaching in the cited prior art of providing a rate of change of voltage detection device and there is further no teaching of activating a current generator for introducing a current to the parasitic capacitance to prevent the parasitic capacitance from drawing current from the input signal responsive to detection of a rate of change of a positive edge of said input signal by said device. Similar limitations have been included in new method claim 33 as well as new apparatus claim 34. Apparatus claims 35 - 37

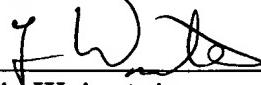
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which depend from apparatus claim 34 further recite that the correction circuit comprises a current source coupled to a first transistor a common terminal between the current source and the first transistor coupled to an output of the detection circuit and the current generating circuit further comprising a second transistor coupled to said common terminal through a third transistor. Claim 36 further recites the second transistor as being a PMOS transistor and said third transistor is an NMOS amp transistor. Claim 37 recites the detection circuit as a capacitor coupled between said parasitic capacitance and said common terminal. These features are neither taught nor remotely suggested by the cited prior art relied upon by the Examiner and it is submitted that new claims 32-37 patentably distinguish over the art together with claims 1-3, 5, 6, 8, 9, 12, 13, 18, 25 and 28-31.

Favorable action is awaited.

Respectfully submitted,

Drapkin et al.

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